



Experimental Studies on Test Pattern Generation for BDD Circuits

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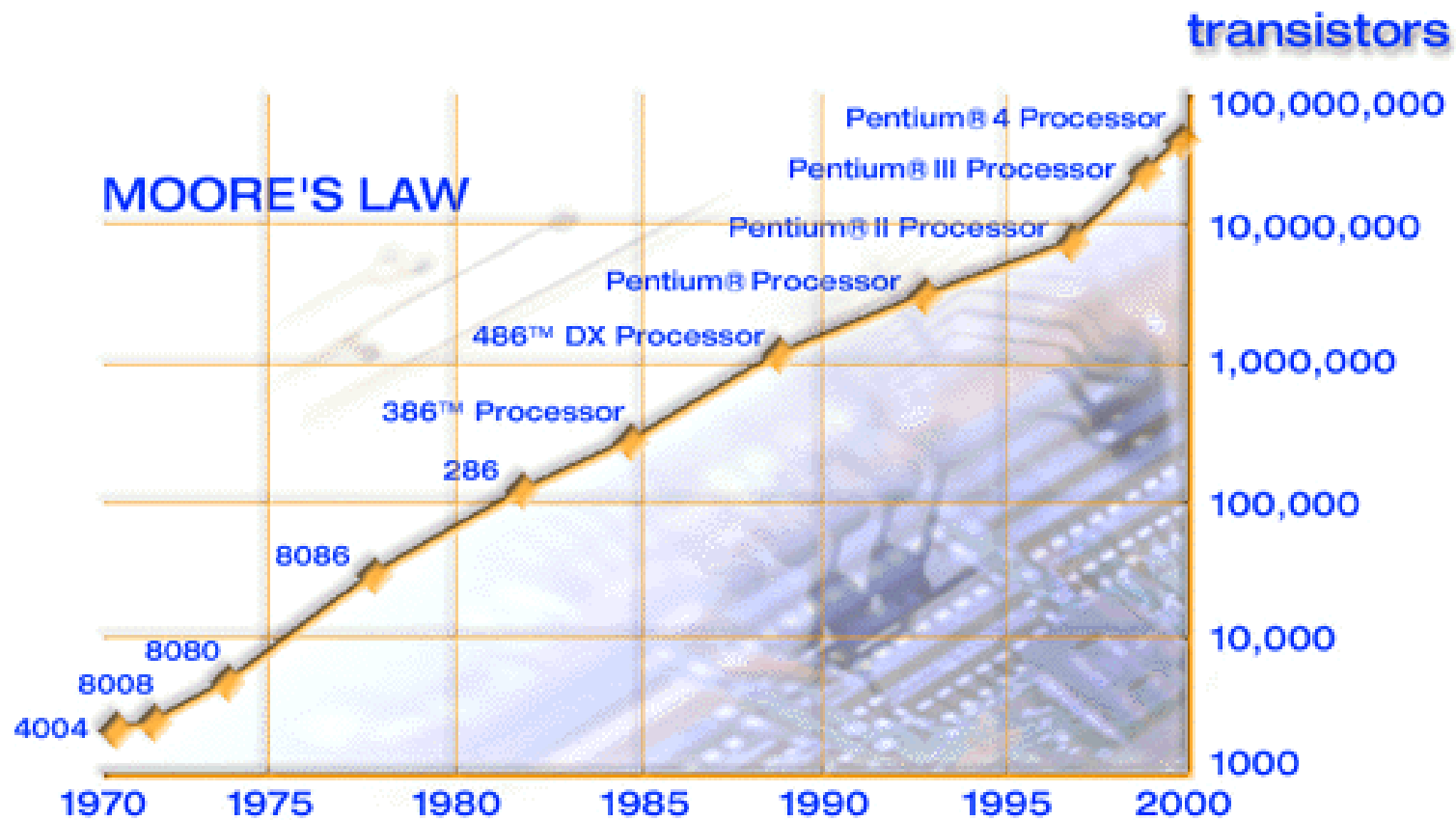


Outline

- Motivation
- BDDs
- BDD circuits
- ATPG tool: TEGUS
- Results
- Conclusions



Motivation(1)





Motivation (2)

- Computer Aided Design (CAD) is necessary to construct complex systems
- Applications in CAD are e.g.
 - Synthesis
 - Design for testability
- ATPG



Motivation (3)

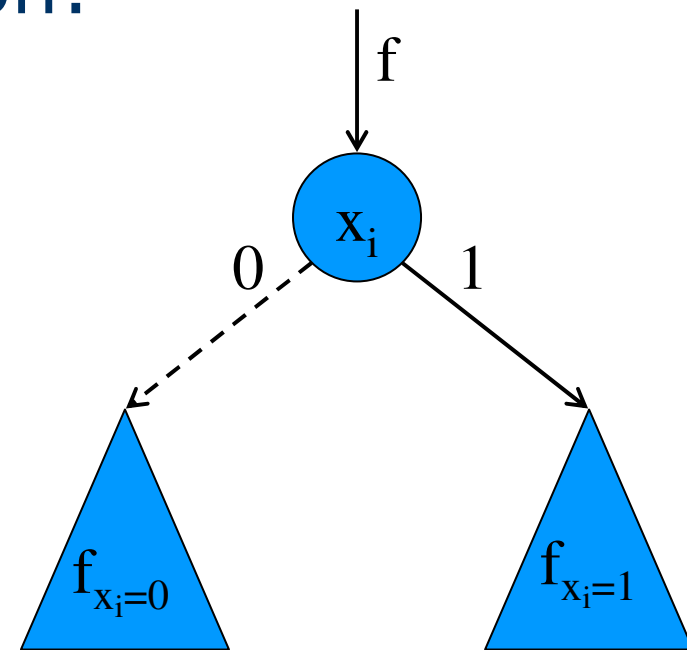
- Binary Decision Diagrams (BDDs)
 - Graphical representation of Boolean functions
 - Widely used in VLSI CAD
- Testability of BDD circuits
 - Simple transformation of BDD circuits to ensure 100% testability for stuck-at faults *and* path delay faults
- **But:** number of test patterns?

Binary Decision Diagrams (BDDs)

- Shannon decomposition:

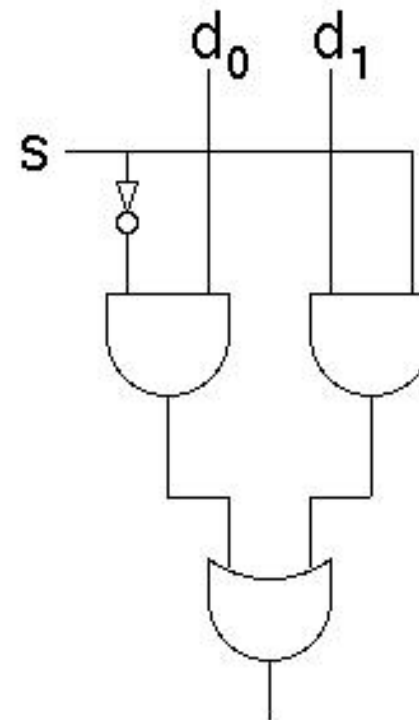
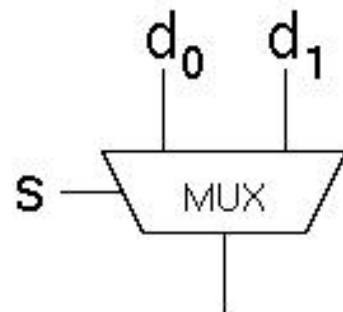
$$f = \bar{x}_i \cdot f_{x_i=0} + x_i \cdot f_{x_i=1}$$

- Terminals: '0', '1'
- Ordered and reduced BDDs
- Reduction and ordering lead to canonicity



BDD Circuits

- Two libraries are considered
 - MUX
 - STD



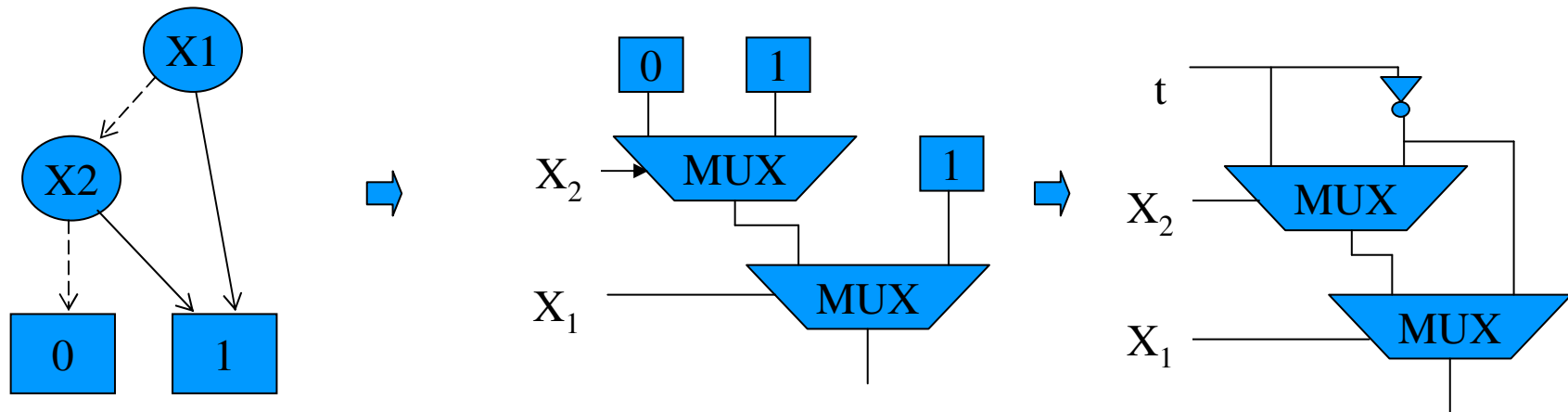


BDD circuits Transformation

- Direct mapping of BDDs
- Each node is substituted by a multiplexor
- Substitute each terminal node by a wire and connect it to a new input t (Drechsler et al., IEEE TCAD, 2004)

Example

$$f(x_1, x_2) = x_1 + x_2$$





ATPG Tool: TEGUS

- SAT based ATPG
- Uses
 - approach as in D-algorithm
 - global implications
 - fault collapsing
 - fault simulation



Experimental Setup

- SUN Fire 280 with 3 Gbyte
- Algorithm integrated into CUDD
- Circuits decomposed into cells from STD library using SIS
- Experiments using TEGUS

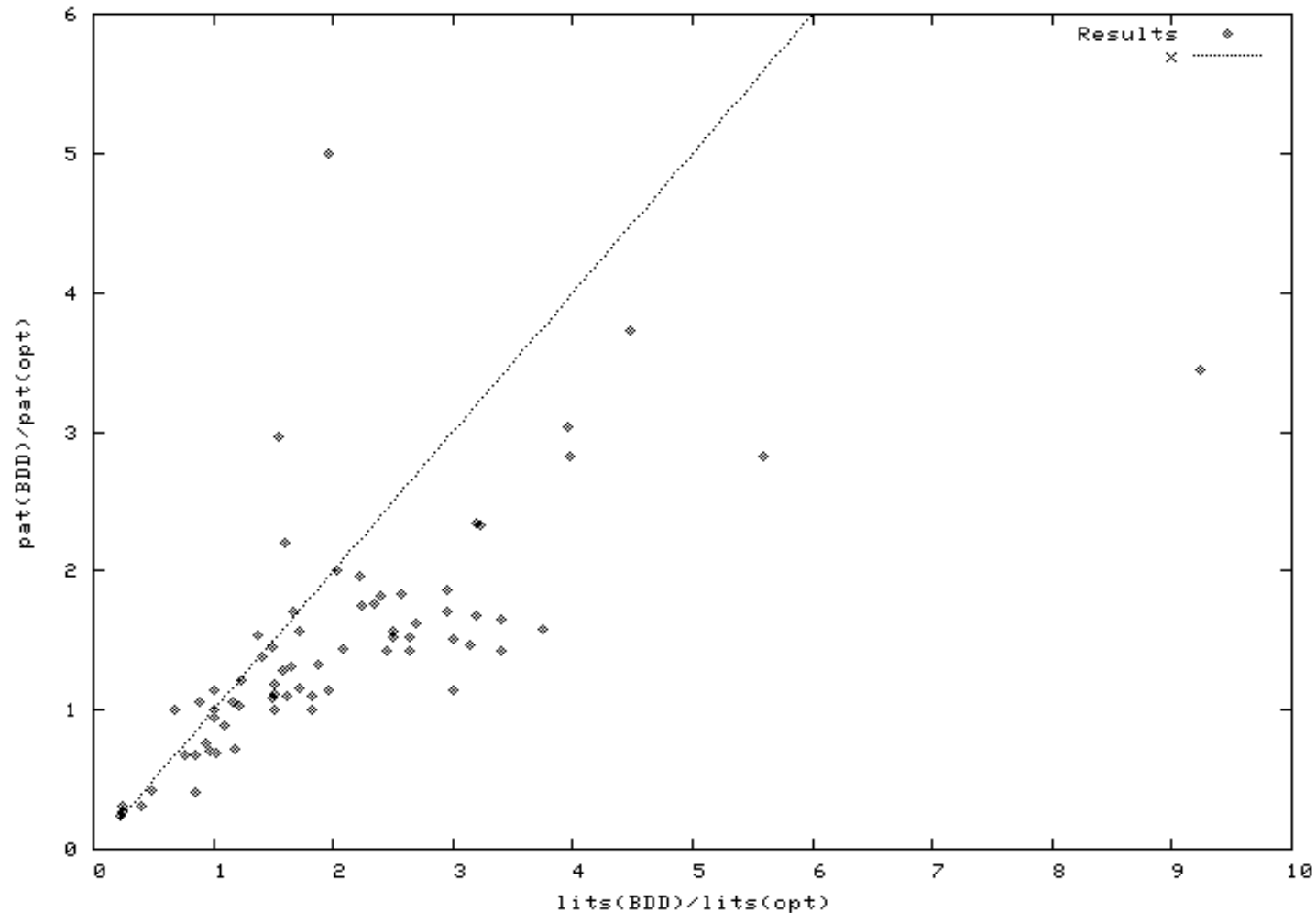


Experimental Results

Circ.	optimized				BDD circuit				$\frac{lits(BDD)}{lits(opt)}$	$\frac{pat(BDD)}{pat(opt)}$
	Lits	Pat.	Ct.	Red.	Lits	Pat.	Ct.	Red.		
5xp1	277	41	228	0	238	28	242	0	0.86	0.68
alu2	700	92	562	13	1124	203	995	0	1.60	2.20
Cht	240	35	315	0	564	62	601	0	2.35	1.77
Vg2	236	62	218	7	493	89	480	0	2.08	1.43
Rd84	614	101	518	6	243	31	247	0	0.39	0.30
t481	812	164	751	9	192	50	206	0	0.23	0.30



Relation Between Test Patterns and Literals





Conclusions

- Full testability can be achieved
 - Moderate overhead in circuit size
 - Small number of additional test patterns

- Better results can be expected for multiplexor based design styles